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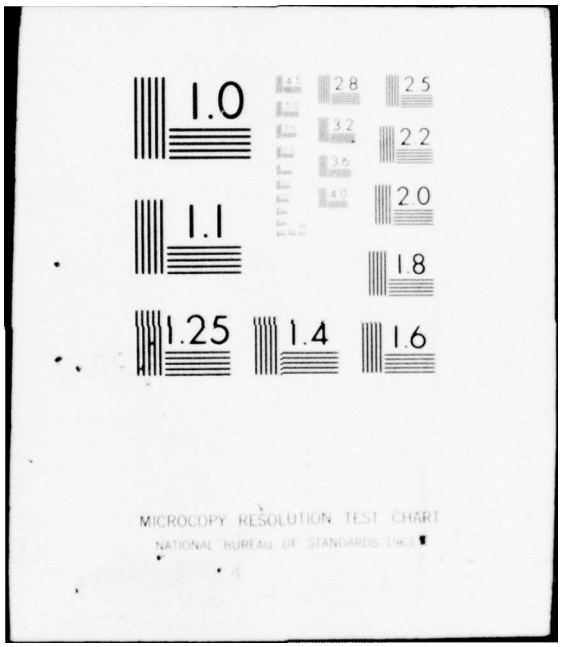
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SECTION I

ABSTRACT

Wafer fabrication for sample generation has been completed on all integrated-circuit types. The critical experiments completed to data have resulted in the unification of the COSMOS and bipolar metallization processes, optimization of the gold-interconnect thickness, development of a suitable COSMOS silicon nitride-silicon oxide gate dielectric, and optimization of the gold bond-pad height. The platinum layer thicknesses required for an effective diffusion barrier and platinum silicide formation have been determined.

Preliminary reliability testing has been initiated and data generated on a 250 deg C bias-life test. A failure mechanism associated with high temperature life tests and epoxy molding compounds has been identified; packaging techniques designed to eliminate this failure mode are being investigated.

A preliminary cost baseline has been established.

SECTION II
PURPOSE

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve semiconductor reliability which will meet military requirements without a severe cost penalty.

The approach to achievement of the goals of this program will be the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program will be carried out in three phases. During Phase I of the program - Sealed-Chip Process Utilization - three major tasks will be accomplished:

(a) Process feasibility - in which the required photomasks will be generated using existing masks to the maximum extent possible. Then, small quantities of each device type will be made to assure that the masks and processes are available for the production runs of Phase II. Also, each device type will be made using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process development - in which the processes required to the fabricate the eight integrated-circuit types to be produced in Phase II will be defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system will be used to achieve chip hermeticity and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer will be

applied for protection of the metallization. A series of experiments will be carried out at each critical processing step to assure repeatability. Real-time indicators and accelerated life tests will be used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated assembly - in which the technology to be used in Phase II will be defined and documented. The effect of assembly process parameters on cost and yield will be assessed. Bonding tapes and lead-frames compatible with each of the device types will be designed and fabricated. A number of devices of each type will then be assembled using the automated assembly system. Reliability will be continually monitored by real-time indicators and accelerated life tests.

At the conclusion of Phase I, the photomasks, wafer process, and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase will have been defined and documented and sample devices of each type will have been fabricated. Additionally, preliminary reliability data will have been generated to demonstrate the soundness of the chosen approach.

At this time, the production runs of Phase II will be undertaken.

Phase II - Fabrication

The low-cost high-reliability device fabrication phase of the program will involve significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits will be constructed in both plastic and ceramic packages. This will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two process will be defined and documented. The utilization of existing equipment and mask sets will be demonstrated, and the

cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions at wafer probe and final test will be used to monitor the production run and to assure process reproducibility. All devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and assembled.

Phase III - Reliability

The reliability of the devices produced in Phase II will be demonstrated. The conventional aluminum-metallized integrated circuits, packaged and tested to military high-reliability requirements, will be used as the baseline from which to appraise the new process developed under the program. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

SECTION III

GENERAL FACTUAL DATA

PERSONNEL

NAME	HOURS
T.R. DeShazo	206
W.N. Lewis	205
T.J. McGrath	8
R.R. Massa	203
S.C. Ahrens	220
F.R. Luberecki	357
T.V. Sikins	158
A.G. Rivera	237
B.B. Levin	236
F.E. Scheline	178
M.A. Polinsky	195
C.L. Tollin	199
F. Boryszewski	24
R.K. Reusch	170
K.J. Orlowsky	144
T. Kamprath	98
R.D. Baird	135
H. Michno	252
F.P. Chiovarou	205
M.J. Tedesco	8
Total	3646

SECTION IV

Detailed Factual Data

Technical Discussion

A. Initial Sample Generation

During this reporting period, the initial wafer fabrication was completed on all integrated-circuit types. The successful development of magnetron sputtering for the deposition of titanium and platinum has resulted in a common metallurgical system for both COSMOS and bipolar circuits. The status of each circuit with regard to the testing programs, sample characterization and high-low temperature testing is shown in Table IV-1.

B. Results of Electrical Characterization

A summary of electrical data taken on types 5420, 54S20, 5470, 5472 and CD4012B are shown in Tables IV-2 through IV-6.

C. COSMOS Gate Dielectric Development

The composite SiO_2/Si_3N_4 gate dielectric required for trimetal COSMOS integrated circuits has been finalized. Circuits were fabricated with 200Å and 400Å Si_3N_4 layers on 900Å and 800Å SiO_2 layers, respectively, and subjected to bias-life testing. The results are summarized in Table IV-7. Based on these data, a dielectric of 900Å of SiO_2 and 200Å of Si_3N_4 was chosen for the COSMOS circuits.

The integrity of the Si_3N_4 film was tested by two techniques, capacitor fabrication and radioactive sodium penetration. The capacitor fabrication test was conducted as follows:

Table IV - 1 — Device Status Review

TA #	Description	Test Program	Sample Characterization	100-Unit Hi-Low Temp. Characterization
1. TA10151	"5420" Dual 4-Input NAND Gate	C	C	C
2. TA10152	"54S20" Schottky Dual 4-Input NAND Gate	C	C	C
3. TA10153	"5470" Edge-Triggered J-K Flip-Flop	C	C	C
4. TA10154	"5472" Master Slave J-K Flip-Flop	C	11/15	12/15
5. TA10155	"CD4012B" COS/MOS Dual 4-Input NAND Gate	C	C	11/15
6. TA10156	"CD4027B" COS/MOS Dual J-K Flip-Flop	C	11/15	11/30
7. TA10219	"CD4014A" COS/MOS 8-Stage Shift Register	C	11/15	12/30
8, TA10158	"CA741" Operational Amplifier	C	12/1	12/30

C = Complete

Table IV - 2 – TA10151 "5420" Dual 4-Input Gate

Electrical Characteristics

	Typical Measured			Spec. Limit		
	–55°C	25°C	125°C	Min.	Max.	Units
V_{OH}	2.70	2.78	2.8	2.4		V
V_{OL}	0.23	0.26	0.34		0.4	V
V_{IC}		–1.05			–1.5	V
I_{IH1}	8	17	28.8		40	μA
I_{IH2}	12.8	26	41.6		100	μA
I_{IL}	–1.12	–1.2	–1.08	–0.7	–1.6	mA
I_{OS}	–33.4	–33.3	–28.6	–20	–55	mA
I_{CCH}	2.4	2.5	2.26		33	mA
I_{CCL}	7.24	7.6	7.0		10	mA
t_{pHL}	10.2	7.6	6.8	3	24	ns
t_{pLH}	9.4	14.8	25	3	27	ns

Table IV - 3 – TA10152 "54S20" Schottky Dual 4-Input Gate

Electrical Characteristics

	Typical Measured			Spec. Limit		
	–55°C	25°C	125°C	Min.	Max.	Units
V_{OH}	2.66	2.98	3.15	2.5		V
V_{OL}	0.51*	0.450	0.415	0.2	0.5	V
V_{IC}		–0.700			–1.2	V
I_{CEX}	0	2	850*		250	μA
I_{IH1}	0.1	0.1	2.0		50	μA
I_{IH2}	0.0001	0.0001	0.003		1	mA
I_{IL}	–1.70	–1.8	–1.62	–1	–2	mA
I_{OS}	–67	–73	–68	–40	–100	mA
I_{CCH}	6.08	6.4	5.86		8	mA
I_{CCL}	12.7	14.0	13.3		18	mA
t_{pHL}	7.2	6.7	6.8	2	9	ns
t_{pLH}	6.9	6.7	7.8	2	9	ns

* Out of Spec.

Table IV - 4 – TA10153 "5470" Edge-Triggered J-K Flip-Flop

Electrical Characteristics

	Typical Measured			Spec. Limit		
	–55°C	25°C	125°C	Min.	Max.	Units
V_{OH}	2.67	2.99	3.4	2.4		V
V_{OL}	0.29	0.277	0.324		0.4	V
V_{IC}		–1.09			–1.5	V
I_{IL1}	–1.07	–1.15	–0.99	–0.7	–1.6	mA
I_{IH1}	12	22.7	33.8		40	μA
I_{IH2}	16.7	32	48		100	μA
I_{IH3}	18.2	35	48.8		80	μA
I_{IH4}	24.6	48	67.8		200	μA
I_{OS}	–21.9	–25.5	–22.3	–20	–57	mA
I_{CC}	14	14	13		30	mA
f_{max}	15	18	16	7.5		MHz
t_{pLH} (Clear to Output)	19	23	29	5	62	ns
t_{pHL} (Clear to Output)	20	15	17	5	62	ns
t_{pLH} (Clock to Output)	32	30	36	5	62	ns
t_{pHL} (Clock to Output)	29	23	24	5	62	ns

Table IV - 5 – TA10154 "5472" Master Slave J-K Flip-Flop

Electrical Characteristics

	Typical Measured			Spec. Limit		
	−55°C	25°C	125°C	Min.	Max.	Units
V_{OH}	2.64	2.95	3.34	2.4		V
V_{OL}	0.257	0.276	0.349		0.4	V
V_{IC}		−0.98			−1.5	V
I_{IL1}	−1.120	−1.132	−1.009	−0.7	−1.6	mA
I_{IL2}	−2.00	−2.05	−1.88	−1.4	−3.2	mA
I_{IL3}	−1.118	−1.116	−1.016	−0.7	−3.2	mA
I_{IH1}	1.88	3.38	7.6		40	μA
I_{IH2}	0.1	0.1	0.1		100	μA
I_{IH3}	16.4	27.2	44		80	μA
I_{IH4}	16.8	28.0	45.6		200	μA
I_{IH5}	−339	−376	−368	−500	−5[illegible]	μA
I_{OS}	−27	−26.7	−23.2	−20	−5[illegible]	mA
I_{CC}	12.8	13	11.8		20	mA
f_{max}	41	40	32	5		MHz
t_{pLH} (Clear to Output)	6	8	12	5	39	ns
t_{pHL} (Clear to Output)	17	16	17	5	50	ns
t_{pLH} (Clock to Output)	7	9	13	5	39	ns
t_{pHL} (Clock to Output)	17	16	17	5	50	ns

Table IV - 6 – TA10155 "CD4012B" Dual 4-Input NAND Gate

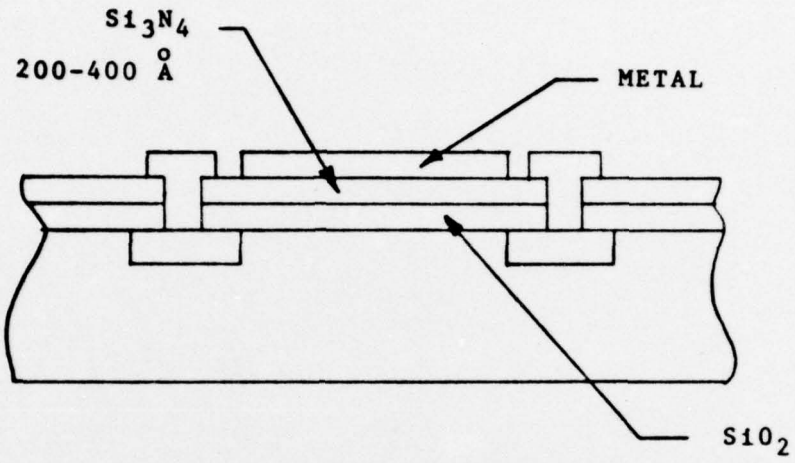
Electrical Characteristics

	Typical Measured				Spec. Limit	
	–55°C	25°C	125°C	Min.	Max.	Units
V_{IC} (Pos)		0.78			1.5	V
V_{IC} (Neg)		–0.71			–6	V
I_{SS}		–0.56	–579		–750	nA
V_{OH1}	4.87	4.85	4.83	4.2		V
V_{OH2}	5.01	5.01	5.00	4.95		V
V_{OH3}	12.13	12.11	12.09	11.25		V
V_{OL1}	0.058	0.06	0.064		0.5	V
V_{OL2}	0.001	0.001	0.004		0.05	V
V_{OL3}	0.072	0.24	0.624		1.25	V
I_{IH1}		0.4			8	nA
I_{IL1}		–0.2			–8	nA
I_{IL2}		–0.02	–5.75		–45	nA
C_i		8.5			12	pF
t_{pHL}		70		15	290	ns
t_{pLH}		55		15	290	ns
t_{THL}		115		40	575	ns
t_{TLH}	102			35	610	ns

Table IV - 7 – COS/MOS Gate Dielectric

Si_3N_4 Thickness Evaluation

Basic Structure Under Evaluation



Operating Life Data for Negative Gate Bias

Conditions	ΔVTN		ΔVTP		Hours
Silicon Nitride Thickness	200 Å	400 Å	200 Å	400 Å	
150°C, 12 V	+0.1	+0.26	–0.12	–0.22	168
125°C, 12 V	+0.12	–	–0.12	–	1000
	+0.13	–	–0.14	–	2000

Operating-Life Data for Positive Gate Bias Show No Change

Conclusions

1. Stable Trimetal COS/MOS Devices can be Fabricated.
2. Stability Improves with Thinner Si_3N_4 Layers.
3. The Mechanism for Instability is Consistent with Electron Conduction Through the Si_3N_4 Resulting in Interface Charging.

1. Si_3N_4 deposition, t = 200Å
2. 5 minute, 25°C etch in buffered hydrofluoric acid
3. Al metallization to form 160 mil^2 capacitors
4. Electrical test

The capacitor yield was approximately 95 percent.

A radioactive-tracer evaluation to determine the effectiveness of the 200Å, deposited silicon nitride film as an alkaline barrier was performed on a test wafer coated with a 200Å layer of Si_3N_4 over a 3000Å layer of SiO_2. A 0.2-mil solution containing 1.31×10^{-6} atoms Na and 4 microcuries Na_{22} was used to coat a nickel electrode, which was then dried under a heat lamp. The wafer was coated with this tracer element by evaporation at a pressure of 10^{-6} torr and subsequently annealed at 600°C for 22 hours. At this point, the surface radioactivity (R) of Na_{22} was determined. The test wafer was then etched to remove approximately 10Å of Si_3N_4, and the surface radioactivity of the fresh surface was determined.

The test wafer was etched three additional times to remove first a total of 30Å, then 50Å, and then 65Å of Si_3N_4. The residual radioactivity as a percentage of R was determined after each etch. The results of this evaluation for samples of silicon nitride from the system used for COSMOS-IC fabrication are shown in Fig. IV-1.

D. Gold Interconnect Thickness Evaluation

Scanning electron microscope evaluation of 1.5-micron-thick gold metallization runs has shown acceptable coverage of oxide steps. The reduction in thickness from the previously used 2.5-micron layers results in reduced mushrooming during plating, improved protective layer coverage, and increased wafer throughput. As a result, the gold interconnect thickness has been standardized at 1.4 to 2.0 microns.

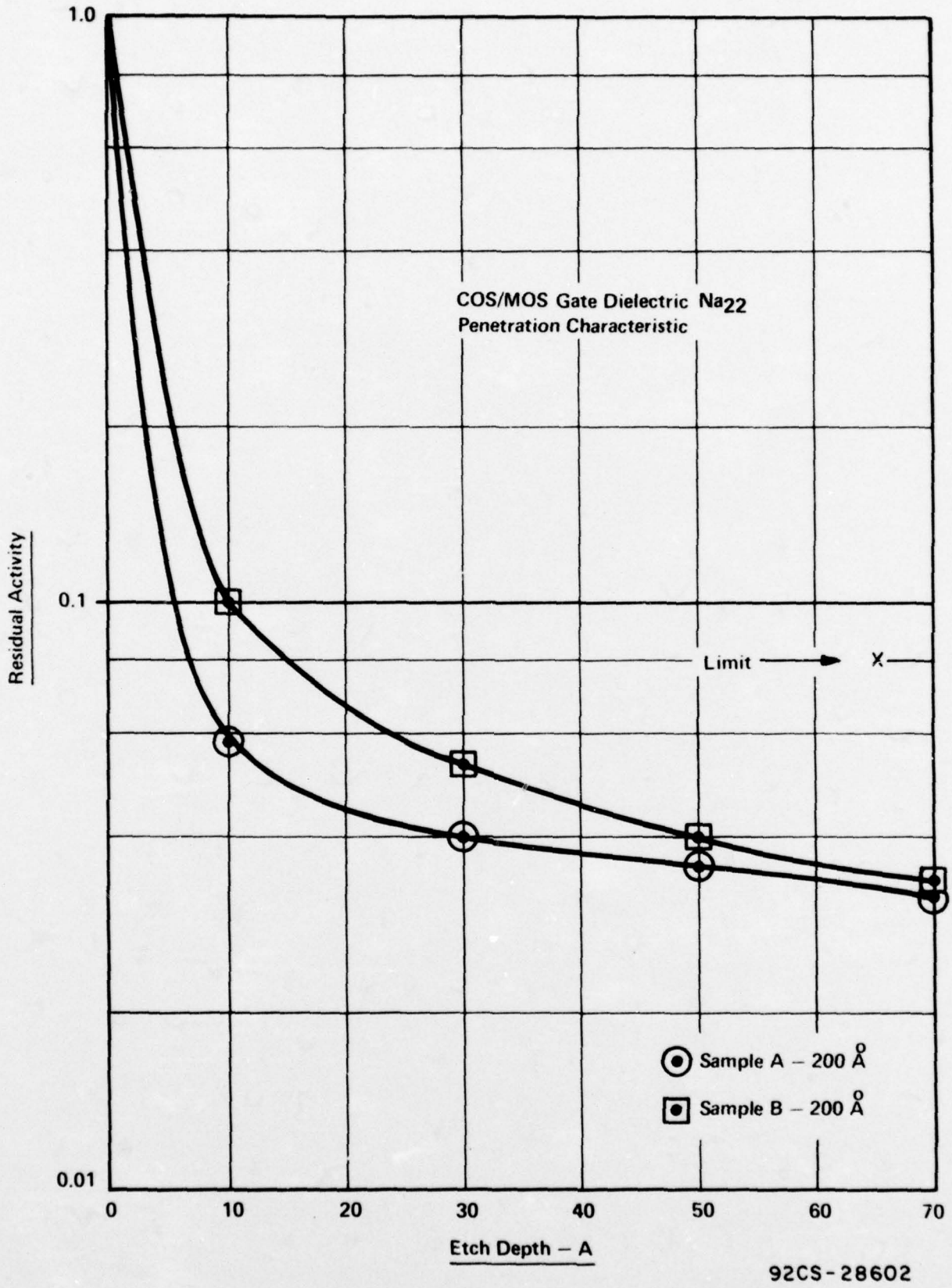


Fig. IV-1 - COS/MOS gate dielectric Na_{22} penetration characteristic.

E. Bond-Pad Height Evaluation

Variations in bond-bump heights between 0.0005-inch and 0.0015-inch have been investigated for optimization in terms of cost, ease of fabrication, and reliability considerations. An eventual decision was made to standardize the 0.001-inch bump height for the following reasons:

- The 0.0005-inch bump height is equivalent to the thickness of the beam-tape polymide support film. The undesirable possibility exists that the polyimide thickness may prevent adequate bump deformation during the inner lead thermocompression bonding.

- The 0.001-inch bump height precludes the eventuality described above. Additionally, as shown in the accompanying metallographic cross-sections, it provides a safety margin, derived from its increased elevation, against the possibility of shorts to the edge of the chip or to the internal metallization.
  Fig. IV-2 illustrates a normally aligned inner lead bond to a 0.001-inch-high bond bump. It will be noted that the deformation accompanying bonding causes the beam to lift away from the edge of the chip - at the left edge of the photomicrograph. Conversely in Fig. IV-3, a beam-to-bump bond is illustrated in which an overlong and misaligned finger extends inboard with respect to the bump. Although there is no edge-short hazard, it is apparent that the overhanging beam has been depressed close to the device metallization. The 0.001-inch-high bump provides an additional margin of safety in this area.

- The bumps are plated into a patterned, dry-film photoresist material requiring exposure and development. This material becomes more difficult to process as its thickness increases, and therefore the use of the 0.0015-inch-thick photoresist required for straight-sided 0.0015-inch-high bumps is considerably less desirable than a thinner resist film.

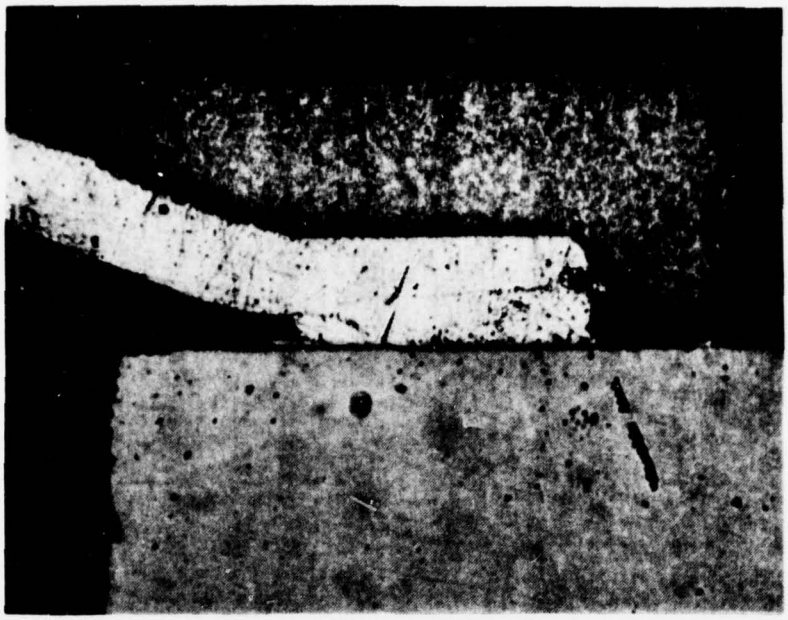


Fig. IV-2 - Normal inner-lead bond, 400X.

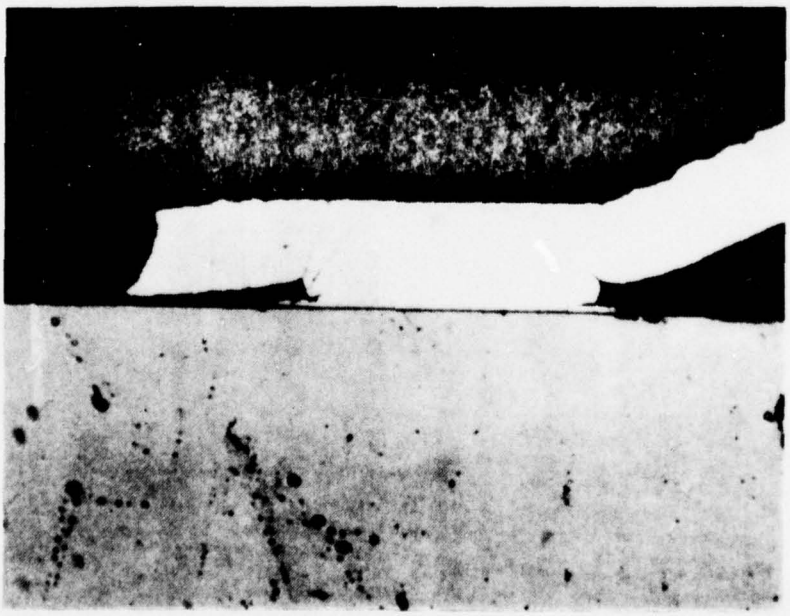


Fig. IV-3 - Misaligned inner-lead bond, 400X.

- The factor of Au costs favors the lowest feasible bump height compatible with device reliability. The 0.001-inch-high bump represents an optimal choice in this area.

F. Platinum Thickness Evaluation-Silicide Formation

CA741 wafers have been fabricated with platinum layers of 500, 800, and 1400Å deposited prior to silicide formation. Wafer electrical testing indicates that yields are adversely affected by increased thicknesses of platinum. The 500Å platinum thickness has been chosen as the standard.

G. Platinum Barrier-Layer Thickness Evaluation

Wafers of CA741 with 1500Å, 2500Å, and 3500Å of Pt for the barrier layer were evaluated with respect to temperature. The lowest temperature at which darkening of the gold was observed on any sample was 400°C. The conclusion drawn from this experiment is that 1500Å of Pt is adequate as a barrier between the titanium and gold layers.

H. Magnetron Sputtering

Trimetal MOS devices have, in the past, been fabricated by means of the titanium palladium gold system. The reasons for this difference is the sensitivity of MOS devices to sputter damage during the Ti Pt deposition process and the high boiling point of platinum, which precludes its use in an evaporation system. It has been found that palladium has the following two major disadvantages as a constituent of a trimetal system, as compared to platinum.

1. Etchability - Processes that successfully etch palladium have also been found to attack palladium silicide; the result is pitted contact regions.

2. Barrier Layer Effectiveness - The purpose of the Pt or Pd layer interposed between the Ti and Au layers is to prevent Ti diffusion to the Au and formation of a relatively high-resistivity intermetallic compound. Pt is superior to Pd as a diffusion barrier.

Furthermore, the successful application of the Ti-Pt-Au metal system to MOS devices would result in a single metallurgical system for all devices in manufacturing, thereby reducing process proliferation and minimizing capital investment.

Magnetron sputtering has been investigated as a technique for the deposition of Ti and Pt layers without the damage normally associated with conventional dc or rf sputtering processes. A model 901 Materials Research Corporation Planar Magnetron Sputtering System was used for this work.

The results of capacitance-voltage bias temperature (CVBT) testing of a magnetron-sputtered Ti film, as deposited, are shown in Fig. IV-4. These curves show an abnormal slope as well as a negative-bias temperature-stress instability. After a 320°C forming gas (90% N2, 10% H2) anneal, however, the sputter-induced damage was eliminated, as shown in Fig. IV-5.

Samples of the CD4012B have been fabricated with both magnetron and rf sputtering. CVBT plots comparing the two systems are shown in Fig. IV-6. The high level of built-in charge and negative-bias temperature instability induced by rf sputtering is apparent in these plots, while the magnetron-sputtered sample showed normal oxide change and no instability.

The threshold voltages of both p- and n-channel MOS devices fabricated by sputtering have been measured. These data are shown in Table IV-8. Sputtering of the Ti-Pt in the rf system resulted in high p-channel threshold voltages and depletion-type n-channel MOS devices; this condition indicates a high level of induced positive charge in the MOS gate dielectric. MOS transistor parameters for the magnetron-sputtered samples were normal. Electrical testing of trimetal COSMOS wafers fabricated with the magnetron-sputtered Ti-Pt wafers has provided yield equivalent to those obtained with

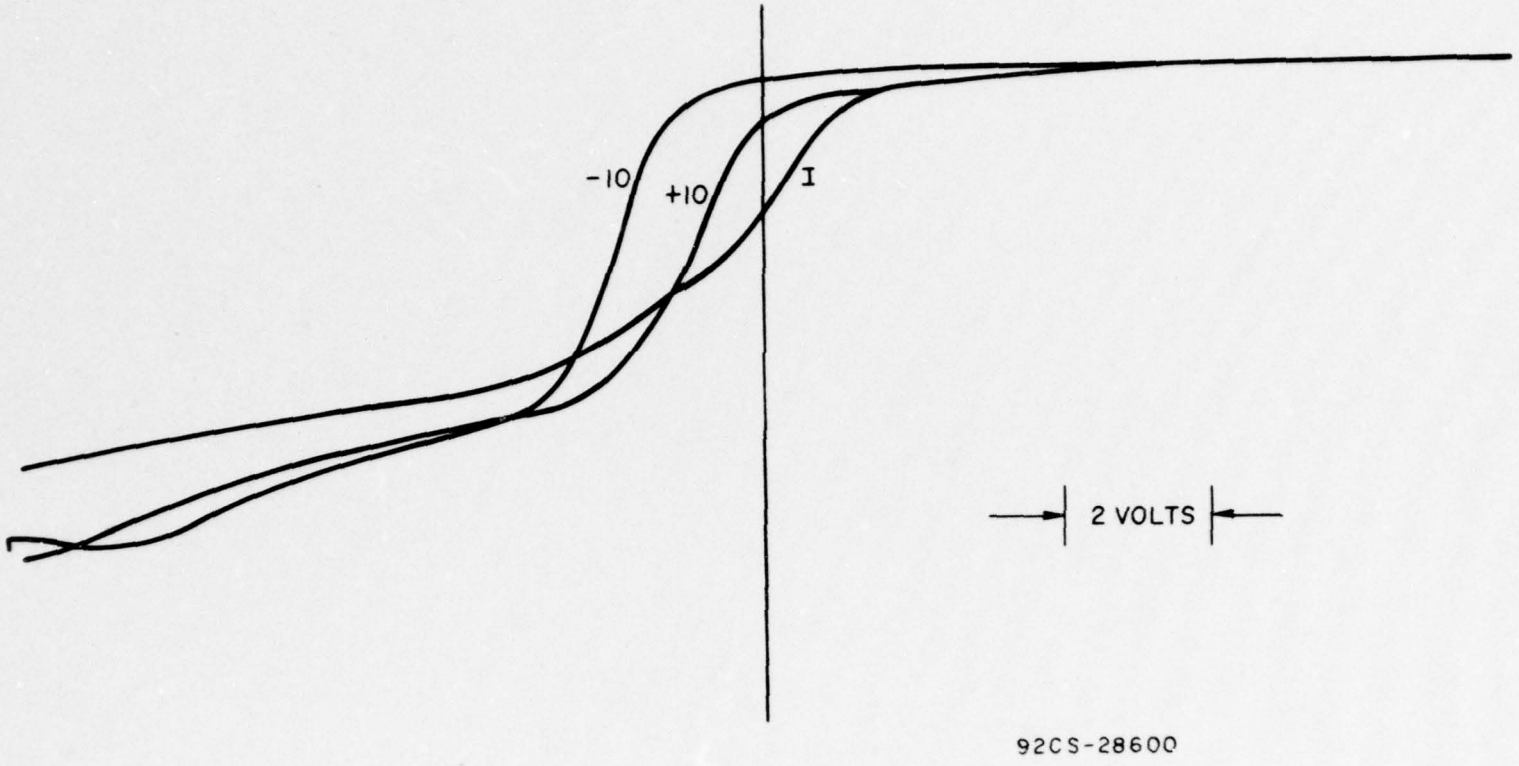


Fig. IV-4 - Bias temperature stress test, magnetron sputtered Ti, not annealed.

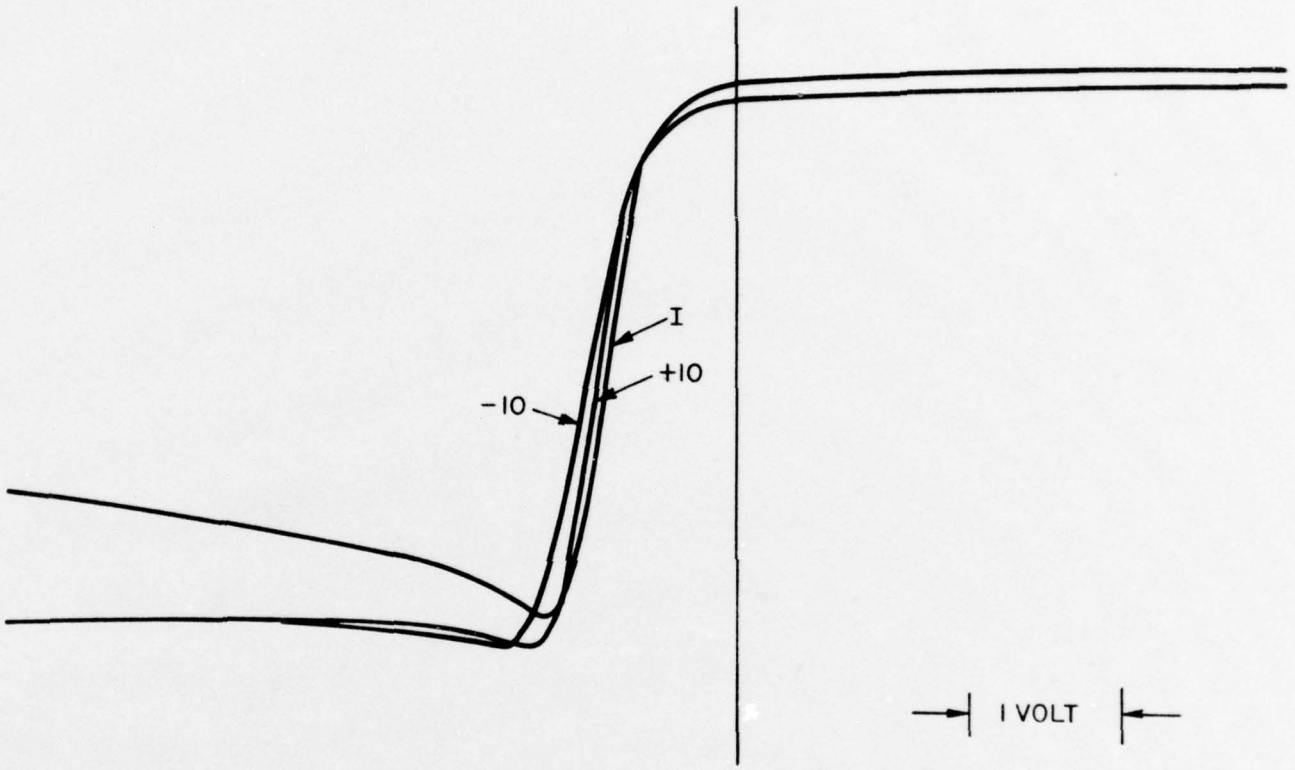


Fig. IV-5 - Bias temperature stress test, sputtered Ti-Pt capacitors after 320°C overnight anneal in forming gas.

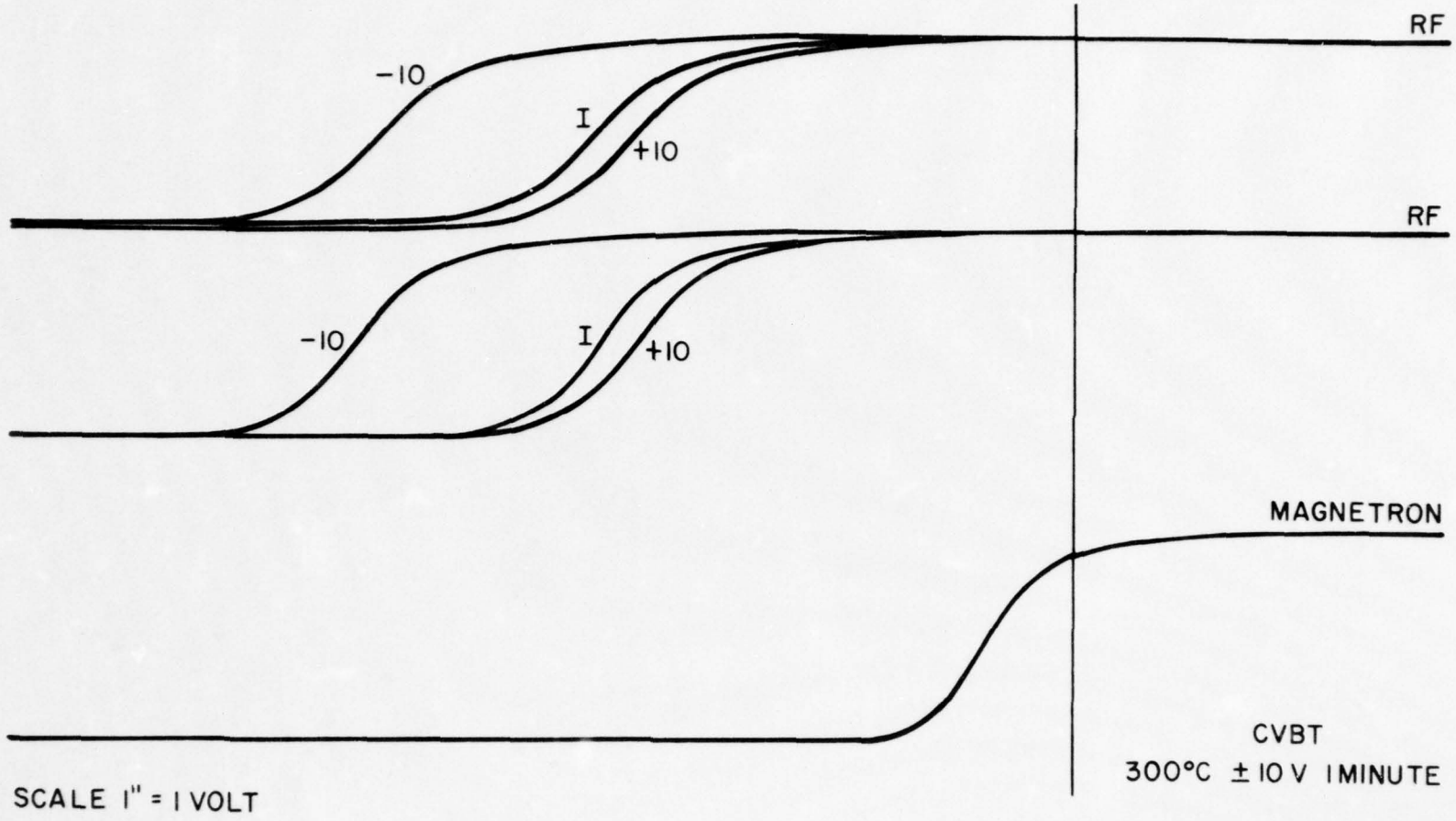


Fig. IV-6 - Magnetron versus rf sputter, CD4012B, after overnight anneal.

Table IV - 8 — Threshold — Voltage Comparison

Ti/Pt-RF Sputtered		Ti/Pt-DC Magnetron Sputtered	
V_{TP} (Volts)	V_{TN} (Volts)	V_{TP} (Volts)	V_{TN} (Volts)
4.06	Depletion	1.58	1.60
4.5	"	1.52	1.68
4.1	"	1.36	1.66
4.0	"	1.32	1.56

conventional aluminum metallized wafers.

As a result of this evalution, the COSMOS circuits now utilize the Ti-Pt-Au metallization system, and a single metallization process has been standardized for all of the integrated circuits fabricated under this contract.

I. Optimization of Metal Overcoat Structure

As reported in the Second Quarterly Report, sputtered silicon nitride films were found to improve the adherence of CVD PSG to gold metallized circuits by protecting the PSG from the deleterious effects of exposure to room atmosphere. However, after prolonged exposure to moist ambients, a degradation in adherence has been observed. This degradation is caused by the non-conformity of the Si_3N_4 film over the CVD PSG film at the edges of metallized areas, an effect confirmed by subjecting sputtered Si_3N_4, CVD PSG overcoated wafers to a chemical etch and observing attack on the edges of the gold metallized areas.

Initial tests of rf-plasma-deposited silicon nitride indicate that these films are conformal over CVD PSG coated gold metallized circuits. A matrix of experiments to determine the optimum overcoat structure has been initiated

J. Platinum Sputter Etch Evaluation

Sputter etching of platinum using gold as an etch mask has the following potential advantages over the standard process.

1. Process simplification and cost reduction.
2. Improved ability to define narrow metal lines. A comparison of the processing steps for the standard and sputter etch processes is shown in Table IV-9.

Table IV - 9 – Chemical-Sputter Pt Etching Comparison

Chemical Etching	Sputter Etching
1. Sputter Ti/Pt	1. Sputter Ti/Pt
2. Pt Photoresist (Shipley)	2. Au 1 Photoresist
3. Pt Etch	3. Au 1 Plate (Interconnects)
4. Photo Removal	4. Au 2 Photoresist (Riston)
5. Au 1 Photoresist	5. Au 2 Plate (Bumps)
6. Au 1 Plate (Interconnects)	6. Photo Removal
7. Au 2 Photoresist (Riston)	7. Sputter Etch Pt
8. Au 2 Plate (Bumps)	8. Ti Etch
9. Photo Removal	
10. Ti Etch	

Initial sputter-etching experiments in an argon plasma have resulted in incomplete removal of the platinum at oxide steps. Other approaches, such as plasma etching and reactive sputter-etching are under investigation.

K. Plasma Si_3N_4 Etch Evaluation

Plasma definition of the CVD Si_3N_4 layer results in process simplification and cost reduction. A comparison of the standard and plasma processes is shown in Table IV-10.

Wafer lots have been processed using the plasma-etch technique. Initial results are satisfactory; however, complete evaluation of parameters and yield is required before this process is standardized.

L. Automated Assembly

Inner lead bonding to the bipolar types has consistently provided pull-strengths at the 50-gram level with beam breaks as the predominant failure mode. Initial results of the CMOS inner-lead-bond pull-strength tests have not been as high or as consistent, and a previously undetected failure mode was observed. This failure mode involved occasional detachment of the bond bump from the device at low pull strengths as a result of cracking of the silicon underlying the bond-pad area.

This type of breakage is shown in Fig. IV-7, which shows that small areas of silicon have been detached from the device under one bump as a result of the pull tests. The fractured surface of the Si is conchoidal in nature, indicating that sharp tension stresses have been applied locally. The source of these stresses is believed to be related to the Ti-Pd-Au metallization applied to the CMOS devices in contrast to the Ti-Pt-Au metallization used for the bipolar devices.

Data have been obtained on CMOS devices with magnetron-sputtered Ti-Pt-Au metallized circuitry. Apparently, the incidence of cracked Si has

Table IV - 10 – Chemical-Sputter Etching Si_3N_4 Comparisons

Standard Etch	Plasma Etch
1. Deposit SiO_2	1. Apply Photoresist
2. Apply Photoresist	2. Etch Si_3N_4
3. Etch	3. Etch SiO_2
4. Remove Photoresist	4. Remove Photoresist
5. Etch Si_3N_4	
6. Etch Top Layer SiO_2 and Contacts	

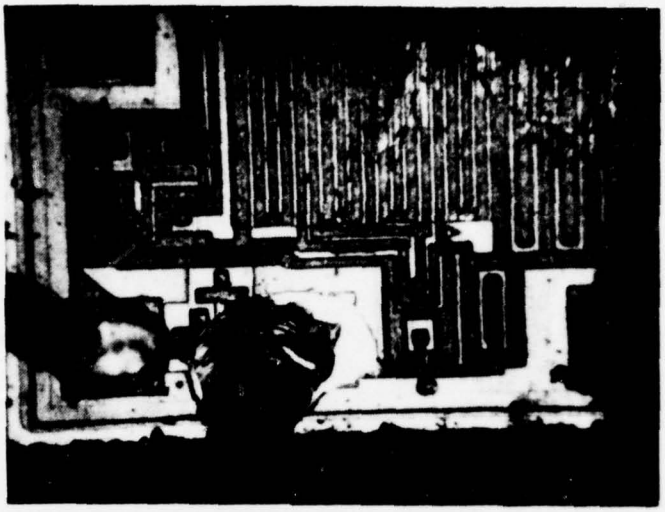


Fig. IV-7 - CD4012B; Ti-Pd-Au metallization. Silicon crack under bump pad on pull testing, 200X.

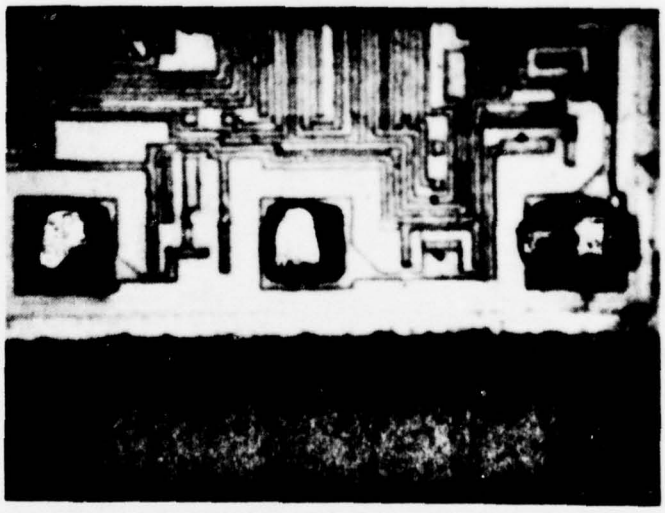


Fig. IV-8 - CD4012B; Ti-Pt-Au metallization. Pull tests yield only beam breaks, 200X.

been completely eliminated, and uniformly high bond strengths prevail. A typical bond-beam break on the CD4012B is shown in Fig. IV-8.

M. Reliability Testing

A summary of 250°C bias-life test data on types CD4012B and 5420 is shown in Table IV-11.

Additional life tests comparing epoxy molding compounds, with and without junction coat, to silicone molding compounds on types CD4012B, CA741 and 5420 have been initiated.

N. Molding Compound Evaluation

The reliability goals of this program, which involve attainment of a failure rate of 0.005%/1000 hours, make it essential that accelerated stress-testing procedures involving exposure of DIP devices to temperatures up to 250°C for prolonged periods be applied. At these elevated temperatures, changes in the electrical and chemical characteristics of the epoxy molding compound have been noted to have a degrading effect upon the device electrical characteristics.

The data in Table IV-12 illustrate the magnitude and characteristics of the problem arising with exposure of epoxy molded DIP's to elevated temperatures. From these data it will be seen that:

- Considerable evidence exists to demonstrate the capability of epoxy-molded devices to withstand exposure to ambient temperatures below 175°C without failure. Failures are first observed when the device temperature reaches 200°C during the 150°C operating-life testing. The failures are primarily the result of electrical leakage and short circuits (test No. 1508).

Table IV - 11 – 250°C Bias Life Summary

	CD4012B				
	Epoxy		Silicone		Epoxy with Junction Coat
Time (Hrs.)	Wire Bond	Auto DIP	Wire Bond	Auto DIP	Auto DIP
48	1/6	1/7	1/6	3/7	–
170	1/6	5/7	1/6	3/7	–
357	6/6	–	1/6	3/7	–
			5420		
48	0/6	1/6	0/6	0/6	–
170	0/6	5/6	0/6	0/6	–
357	5/6	–	0/6	0/6	–

Table IV - 12 – Dip – Automated Assembly
Elevated Temperature Life Test Data

Device (Test No.)	Molding Compound	Beam Tape Construction	Test Conditions	Hours Exposure	Results Fail/Total	% Fail
CA3047 (1508)	Epoxy	3M, Cu on Polyimide	125°C Operating Life	1000	0/19	0
			150°C Operating Life T_j = 200°C	1000	5/40	13
			150°C Storage	1000	0/20	0
			175°C Storage	1000	0/35	0
CA3046 (1600)	Epoxy	3M, Cu on Polyimide	150°C Operating Life T_j = 200°C	48	14/15	95
CA3046 (1602)	Epoxy	3M, Gold Plated Cu on Polyimide	150°C Operating Life T_j = 200°C	48	12/15	85
CA3046 (1562)	Epoxy	Bare Cu No Polyimide	150°C Operating Life T_j = 200°C	168	18/20	90
CA3046 (1604)	Silicone	3M, Cu on Polyimide	150°C Operating Life T_j = 200°C	600	0/10	0
CA3046 (1619)	Epoxy with Silicone Resin Overcoat	3M, Cu on Polyimide	150°C Operating Life T_j = 200°C	660	0/20	0

- The data from Tests 1602 and 1562 indicate that the 150°C (T_J=200°C) operating life failures also occur with the use of bare Cu beam tapes without the polyimide film and with Au/Ni-plated Cu beams on polyimide.

- No failures have been noted with beam-tape bonded devices encapsulated with silicone molding compounds (Test No. 1604).

- No failures have been noted (Test No. 1619) with beam-tape bonded devices overcoated with a silicone resin layer prior to molding into the conventional epoxy compound.

Examination of a considerable number of failed units has disclosed that the failures are a result of the deposition of Cu upon structural surfaces such as the device or the polyimide film adjacent to the device. Examination of the Cu beam tape after failure discloses an etched appearance such as that which results from a corrosive attack; it is apparent that a chemical reaction has taken place between the Cu and the epoxy molding compound at the 200°C device temperature.

The epoxy compounds used for semiconductor encapsulation are extremely complex combinations of resin, hardener, accelerator, filler, release agents and specific fire retardant additives. The compounds have been formulated to obtain optimal characteristics with respect to thermal expansion, glass-transition temperature, residual chemical impurity content, moisture absorption and transmission, and a host of other parameters that permit large-scale fabrication of molded DIP's. The development of these properties has been directed toward devices that operate in the 125°C and 150°C range; there is only minimal information available concerning operation at temperatures in excess of 200°C.

The corrosive attack on Cu at these temperatures results from a chemical change in the molding compound, which provides a source for this attack. The precise nature of this source has not as yet been clearly defined, but it may be postulated that Cl_2, Br_2, NH_3, Sb and other

molding compound constituents are liberated to attack and dissolve Cu, and subsequently to permit its redeposition, which leads to degradation of the device metallization. The mechanical barrier provided by the silicone-resin overcoat has the effect of shielding the Cu from the corrodant material and, therefore, no degradation has been noted when the overcoat is present.

Further investigation is continuing in this area to identify the offending component in the epoxy and subsequently to exclude it or its counterparts from the molding compound.

O. Relative-Cost Comparison

Consideration of all of the applicable cost and reliability factors is essential to the validation of the goals of this program. In order to examine the interrelationship between these factors, a basic view of device processing is required, followed by an analysis of those modifications imposed to attain the necessary reliability levels. It is obvious that the cost of these process changes cannot exceed the program's restrictions of 20-percent over commercial high-reliability types. Discussions with the program management have clearly established the desirability of fulfilling the optimal consideration for the attainment of commercial-type low-cost with requisite military-type high reliability.

Table IV-13 presents relative-cost data for the domestic production of plastic- and ceramic-packaged integrated circuits. The costs are related to yields and cover material and labor. The CA741 14-lead device was chosen to provide the baseline data for the comparison; costs for production levels of 15×10^6 units per year were utilized. In the System I tabulation, both a lidded-alumina, white-ceramic and a two-piece ceramic, frit-sealed package are described. Analysis of this tabulation establishes the following salient points:

- Wafer processing costs are identical through the diffusion and passivation levels.

Table IV - 13 – Relative Cost Comparison

System Number		I		II	III
System Processes	Passivation	SiO_2		SiO_2	Si_3N_4
	Metallization	Aℓ		Aℓ	Trimetal
	Dielectric Overcoat	CVD PSG		CVD PSG	Si_3N_4
	Device Bonding	Wire		Wire	Beam Tape
	Assembly	Manual		Manual	Automated
	Packaging	Hermetic Ceramic		Plastic	Plastic
Relative Cost Factors	Wafer Process Through Passivation	15		15	15
	Metallization	2		2	6
	Dielectric Overcoat	2		2	2
	Separation	11		11	5
	Assembly	White	Frit Seal	48	22
		250	65		
	Encapsulation and Test	38	30	22	22
	Total Relative Cost	318	125	100	72

- Metallization costs for trimetal circuitry and gold bumps are three times those for conventional aluminum metallization, but represent a small part of the total cost.

- Dielectric overcoating costs, whether CVD PSG or plasma-reactor-deposited Si_3N_4, are identical.

- Conventional wafer separation by scribing and breaking introduces yield losses not experienced in the mounted-wafer sawing procedures used for automated assembly and, therefore, yield losses after scribing and breaking are approximately twice those after sawing.

- Assembly costs include those for the package materials. The high costs for the white-ceramic package dominate this area, but are diminished for the frit-sealed unit. Manual wire bonding is considerably more costly than automated assembly, and this is the principal factor in the cost differential between the System II and System III data.

- Both hermetic packages require sealing and inspection not applicable to plastic-encapsulated packages; these additional steps reflected in the higher cost for System I encapsulation and test.

- The cost data for System II were factored to total 100. The data for the others were then compared to these tabulated in descending order.

- Cost for reliability validation are omitted and will be reviewed later.

Analysis shows that the lowest production costs are those associated with the automated-assembly System III, and that its cost ratio to that of System II is 0.72. Since these data are for a relatively low-cost device, further information is presented in Tables IV-14 and IV-15 for more costly devices.

Table IV - 14 – Comparision of Yield-Related Device Costs – 14 Lead						
Cost Factors	Basic CA741 Device Cost		Double Device Cost		Quadruple CA741 Device Cost	
	System II	System III	System II	System III	System II	System III
Wafer Process	15	15	30	30	60	60
Metallization + Overcoat + Separation	15	13	15	13	15	13
Assembly + Encapsulation	70	44	70	44	70	44
Total	100	72	115	87	145	117
Ratio	0.72		0.76		0.81	

Table IV - 15 – Comparision of Assembly-Related Device Costs – 28 Lead						
Cost Factors	Basic Device Cost		Double Device Cost		Quadruple Device Cost	
	System II	System III	System II	System III	System II	System III
Wafer Process	15	15	30	30	60	60
Metallization + Overcoat + Separation + Encapsulation	37	35	37	35	37	35
Assembly	96	22	96	22	96	22
Total	148	72	163	87	193	117
Ratio	0.49		0.53		0.60	

The basic assumption for the devices used for review in Table IV-14 is that the devices are intended for 14-lead packages, and that the increased cost is related to such yield factors as chip size, circuit complexity, and electrical requirements. The data indicate that, as the cost of the chip increases, with other costs remaining static, the cost advantages accruing to automated assembly decrease in comparison to those for manual wire bonding.

An additional vital factor to be considered in evaluating device costs is that related to assembly. Table IV-15 presents data for the basic, double, and quadruple yield-related device costs as they are affected by an increased number of bonding sites. For a 28-lead DIP, the manual wire-bond assembly costs will be doubled compared to those for the 14-lead DIP considered above. However, since all bonds are made simultaneously in automated assembly, there are no additional costs for this procedure.

Analysis of Table IV-16, which summarizes data from both of the proceding tables, shows that:

- Automated assembly of a basic, 14-lead, low-cost device offers a cost advantage ratio of 0.72.

- Automated assembly of yield-related, costlier devices diminishes this cost advantage.

- Automated assembly of assembly-related, costlier devices enhances this cost advantage.

Table IV - 16 – Cost Data Summary

Number of Leads	Basic Device		Double Cost Device		Quadruple Cost Device	
	System II	System III	System II	System III	System II	System III
14	100	72	115	87	145	117
28	148	72	163	87	193	117

System III/System II Ratio Summary

Number of Leads	Basic Device	Double Cost Device	Quadruple Cost Device
14	0.72	0.76	0.81
28	0.49	0.53	0.60

SECTION V
CONCLUSIONS

1. A gate dielectric composed of 900Å SiO_2 and 200Å Si_3N_4 results in stable COSMOS trimetal integrated circuits.

2. Bond pads 1.0 mil in height are optimum in terms of cost, ease of fabrication, and reliability.

3. A platinum layer of 1500Å provides an adequate barrier to Ti-Au diffusion up to 400°C.

4. Magnetron sputtering provides a technique for the fabrication of trimetal MOS devices using the titanium-platinum-gold metallization system.

5. Sputtered Si_3N_4 layers do not provide conformal coverage of metal lines.

6. The titanium-platinum gold metallization system eliminates the low bond pull-strength problem observed on COSMOS devices fabricated with titanium-palladium-gold.

7. Accelerated, high-temperature (>200°C) life tests cause changes in the electrical and chemical characteristics of epoxy molding compounds; these changes have a degrading effect upon device characteristics.

SECTION VI

PROGRAM FOR THE NEXT INTERVAL

1. Develop the process required for the plasma deposition of Si_3N_4 overcoat layers.

2. Complete the electrical characterization of all types.

3. Continue evaluation of platinum sputter etching.

4. Complete the evaluation of plasma Si_3N_4 processing.

5. Generation of optimized samples.

6. Reliability testing of preliminary and optimized samples.

7. Document materials, masks, and processes for Phase II device fabrication.

8. Refine the cost baseline to include reliability testing.

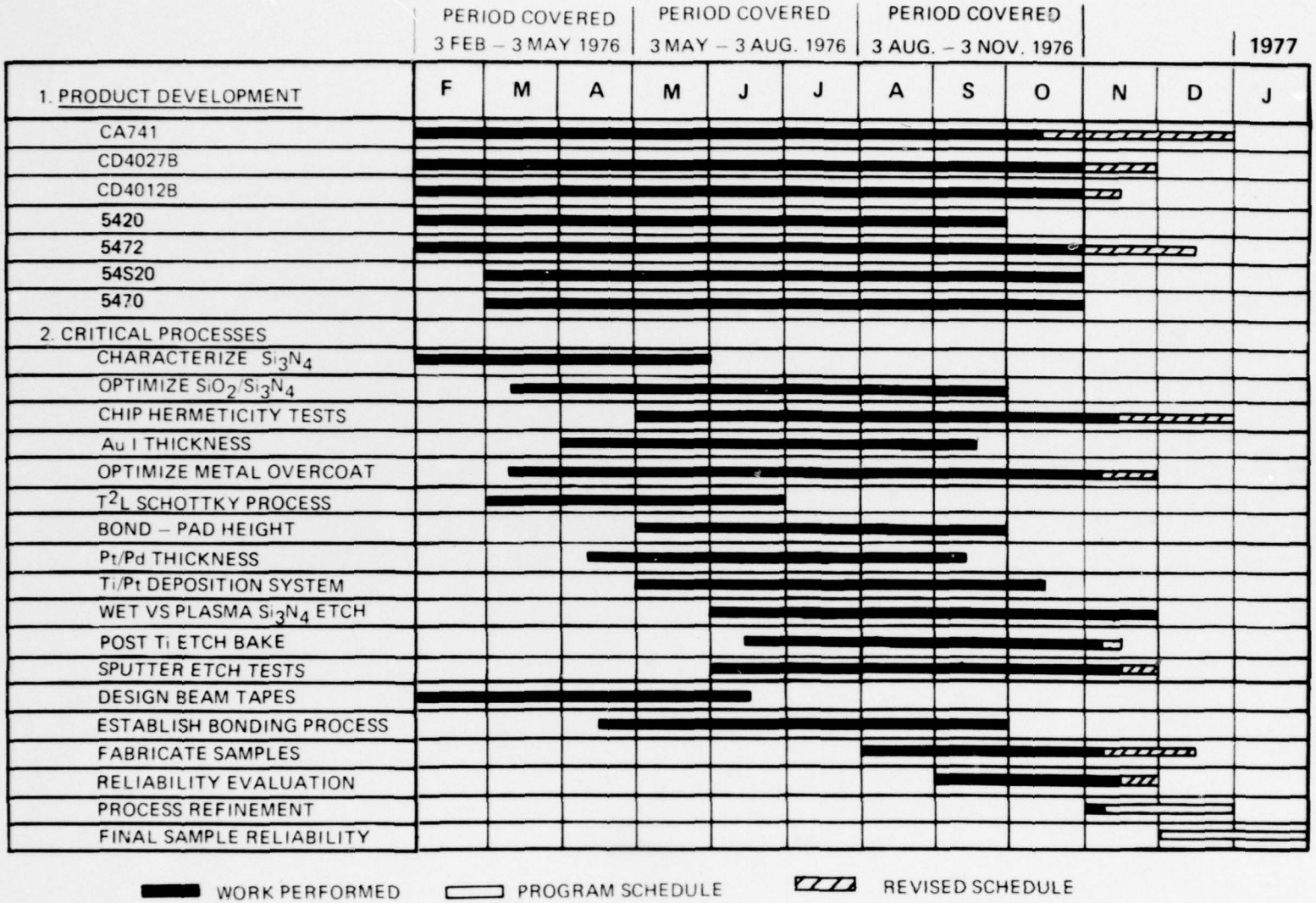


Figure VI-1 - Project performance and schedules. 92CS-28601

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